REMARKS

In the outstanding Office Action, the Examiner has rejected Claims 1-33. Claims 1, 17 and 27 have been amended. Claims 2, 18 and 29 have been cancelled. Claim 34 has been added. No new matter has been added. Thus, the new set of claims are presented for further examination. Reconsideration and allowance of all claims in light of the present remarks is respectfully requested.

Rejections Under 35 U.S.C. § 102(b)

The Examiner has rejected Claims 1-2, 14-18, 20, 25, 27-33 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,118,161 to Chapman, et al.

The Examiner stated that Chapman "teaches the claimed invention in that it discloses a method of forming a FinFET device comprising: ... forming a disposable gate 134 (corresponding to the claimed dummy gate) on the active area (Fig. 22 and col. 4, lines 51-60); forming source/drain regions 110/112 within the active area, the source and drain regions being self aligned to the disposable gate 134 (col. 4, lines 60-65) ... ."

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053.

Claims 1 and 17

Amended Claim 1 recites a method of forming a fin field effect transistor (FinFET) device, comprising, *inter alia*, "forming at least one dummy gate on at least one of the active areas, wherein the at least one dummy gate extends beyond the at least one active area so as to form a connection with another dummy gate ... ."

With respect to Chapman, the active area, i.e., the semiconductor film (106) in which the transistors are made, and the disposable gate 134 are defined using the same layer. *Chapman at col. 6, lines 45-61; Figs 20-22.* As shown in Figure 20 of Chapman, the pad oxide 132 and nitride 130 is used to first pattern the semiconductor layer 106 to define the active area. *Col. 6, lines 55-58.* As shown in Figure 22, this stack is then patterned a second time to define the disposable gate 134, (*col. 6, lines 59-61*), which is inherently self aligned to the active area.

Chapman at col. 4, lines 51-60, in reference to Figure 12 and as cited by the Examiner, discusses only the formation of a disposable gate 134 without any detail as to how the

semiconductor layer 106 is patterned. The only description provided in Chapman with regard to patterning is in regard to Figure 20 as discussed above, and there is no teaching of an alternative to the method discussed in reference to Figure 20.

The double use of the stack 132/130 as described by Chapman *does not allow* the dummy gate 134 to extend beyond the at least one of the active areas as recited in Claim 1. The extension recited in Claim 1 allows for a dummy gate which is common to two FinFET devices as shown, for example, in Applicant's Figure 1.

As Chapman fails to describe, either expressly or inherently, every element as recited in Claim 1, Applicant respectfully submits amended Claim 1 for further review as patentable subject matter.

The CMOS circuit of amended Claim 17 comprises at least two active areas formed in a semiconductor layer, the at least two active areas insulated from each other by field regions; each active area comprising at least one fin field effect transistor (FinFET) device; and each of the at least one FinFET device comprising a source and a drain formed in the semiconductor layer, and a cavity formed in between the source and the drain and common to each FinFET, with a semiconductor fin formed in the semiconductor layer and extending in the cavity from the source to the drain."

An exemplary final device structure is illustrated in Applicant's Figure 1 and described at numbered paragraph [0033] of Applicant's specification, wherein the gate 24 is common to the transistor 40 formed on the left active area and to the transistor 41 formed on the right active area 4. An exemplary discussion of the patterning of the dummy gate and creation of an open cavity as recited in Claim 1 are provided in Applicant's specification, for example, at numbered paragraphs [0038], [0045], [0047], and [0048].

In reference to the discussion above regarding Chapman's double use of the stack 132/130 and the inherent structure which *does not allow* the dummy gate 134 to extend beyond the at least one of the active areas, Chapman accordingly fails to describe a cavity formed in between the source and the drain and common to each Fin FET, with a semiconductor fin formed in the semiconductor layer and extending in the cavity from the source to the drain, as recited in Claim 17.

As Chapman fails to describe, either expressly or inherently every element as recited in Claim 17, Applicant respectfully submits Claim 17 for further review as patentable subject matter.

Claims 27 and 34

Amended Claim 27 recites a method of manufacturing a complementary metal-oxide semiconductor (CMOS) circuit, the method comprising, *inter alia*, "forming at least one dummy gate on at least one of the active areas and at least one gate on an active area other than the at least one of the active areas; forming source and drain regions within the active areas, the source and drain regions being self aligned respectively to the dummy gate and to the gate ... ."

New Claim 34 recites a method of forming a FinFET device and at least one planar FET device, comprising, *inter alia*, "forming at least one dummy gate on at least one of the active areas and at least one gate on an active area other than the at least one of the active areas ... ." Claim 34 recites features similar to those recited in Claim 14 as examined.

Regarding Claim 27, forming at least one gate on an active area other than the active area(s) on which a dummy gate is formed is described, for example, in Applicant's specification at numbered paragraphs [0039], [0045], and [0054]. The method of Claim 27 allows combining in a standard planar CMOS technology the formation of a FinFET with a standard planar transistor and/or a replacement gate transistor by forming at least one dummy gate and at least one gate on active areas of the semiconductor layer.

The word "planar" is used to distinguish standard bulk devices from the FinFET devices which are formed using this disposable gate process. In this respect the device illustrated in Chapman's Figure 8 is not a planar device but a FinFET. A definition of planar devices is provided at numbered paragraph [0004] of Applicant's specification. Chapman's description at col 3, lines 24-26 also distinguishes between the FinFET disclosed by Chapman and standard bulk CMOS devices.

Even if the "standard bulk CMOS transistor" recited in Chapman at col 3, lines 24-27 is to be read as "a standard bulk (i.e. prior art) transistor suitable for use in a CMOS circuit", as suggested by the examiner at page 3, para. 2 of the Office Action, Chapman does not describe nor teach a CMOS circuit as recited in Claim 27, nor how to create such a CMOS circuit comprising at least one p-type FinFET and one n-type FinFET as recited in Claim 30, nor how a combination can be made of a bulk/planar FET with a FinFET as recited in Claim 34.

Thus, as Chapman fails to describe, either expressly or inherently, every element as recited in each of Claims 27 and 34, Applicant respectfully submits these claims for further review as patentable subject matter.

With respect to the dependent claims, because these claims depend from patentable independent claims, pursuant to 35 U.S.C. § 112, ¶ 4, they incorporate by reference all the limitations of the claim to which they refer. It is therefore submitted that these claims are in condition for allowance at least for the reasons expressed with respect to the independent claim, and for their other features.

Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 3-13, 19, and 21-24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,118,161 to Chapman, et al. in view of U.S. Patent No. 6,583,469 to Fried, et al.

Because these claims depend from patentable independent claims, pursuant to 35 U.S.C. § 112, ¶ 4, they incorporate by reference all the limitations of the claim to which they refer. It is therefore submitted that these claims are in condition for allowance at least for the reasons expressed with respect to the independent claim, and for their other features.

New Claim

Claim 34 is similar to original Claim 14 and recites patentable subject matter as discussed above.

Conclusion

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. Accordingly, amendments to the claims for patentability purposes pursuant to statutory sections 102, and/or 103, the reasons therefore, and arguments in support of the patentability of the pending claim set are presented above. In light of these amendments and remarks, reconsideration and withdrawal of the outstanding rejections is respectfully requested.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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